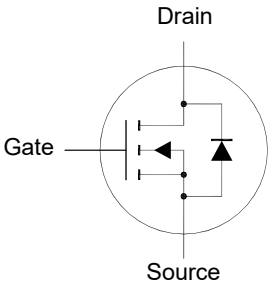
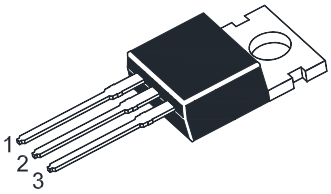
WPCT65N310-HAF

N-Channel Enhancement Mode MOSFET





1.Gate 2.Drain 3.Source
TO-220FB Plastic Package

Features

- Low $R_{DS(on)}$
- Low Gate Charge
- Halogen and Antimony Free(HAF), RoHS compliant

Application

- DC-DC converters
- Lighting
- Hard / Soft switching topology

Key Parameters

Parameter	Value	Unit
BV_{DSS}	650	V
$R_{DS(ON)}$ Max	310 @ V_{GS} = 10 V	mΩ
$V_{GS(th)}$ typ	3	V
Q_g typ	25 @ V_{GS} = 10 V	nC

Absolute Maximum Ratings (at T_a = 25℃ unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage		V_{GS}	± 30	V
Drain Current	T_c = 25℃ T_c = 100℃	I_D	9 5	A
Peak Drain Current, Pulsed [1]		I_{DM}	35	A
Avalanche Current		I_{AS}	4	A
Single-Pulse Avalanche Energy [2]		E_{AS}	632	mJ
Power Dissipation	T_c = 25℃	P_{tot}	62.5	W
Operating Junction and Storage Temperature Range		T_j, T_{stg}	- 55 to + 150	℃

Thermal Characteristics

Parameter	Symbol	Max.	Unit
Thermal Resistance from Juntion to Case	$R_{\theta JC}$	2	℃/W
Thermal Resistance from Juntion to Ambient	$R_{\theta JA}$	50	℃/W

[1] Pulse Test: Pulse Width ≤ 100 μs, Duty Cycle ≤ 2%, Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$ = 150°C.

[2] Limited by $T_{J(MAX)}$, starting T_J = 25 °C, L = 79 mH, R_g = 25 Ω, I_D = 4 A, V_{GS} = 10 V.

Winning Team
互創國際

Dated: 23/12/2020 Rev: 01

Characteristics at T_a = 25℃ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit
STATIC PARAMETERS					
Drain-Source Breakdown Voltage at I_D = 250 µA	BV_{DSS}	650	-	-	V
Drain-Source Leakage Current at V_{DS} = 650 V	I_{DSS}	-	-	1	µA
Gate-Source Leakage Current at V_{GS} = ± 30 V	I_{GSS}	-	-	± 100	nA
Gate-Source Threshold Voltage at V_{DS} = V_{GS}, I_D = 250 µA	$V_{GS(th)}$	2	-	4	V
Drain-Source On-State Resistance at V_{GS} = 10 V, I_D = 7 A	$R_{DS(on)}$	-	250	310	mΩ
DYNAMIC PARAMETERS					
Forward Transconductance at V_{DS} = 5 V, I_D = 7 A	g_{fs}	-	8	-	S
Gate resistance at V_{DS} = 0 V, V_{GS} = 0 V, f = 1 MHz	R_g	-	1.4	-	Ω
Input Capacitance at V_{DS} = 100 V, V_{GS} = 0 V, f = 1 MHz	C_{iss}	-	824	-	pF
Output Capacitance at V_{DS} = 100 V, V_{GS} = 0 V, f = 1 MHz	C_{oss}	-	54	-	pF
Reverse Transfer Capacitance at V_{DS} = 100 V, V_{GS} = 0 V, f = 1 MHz	C_{rss}	-	7	-	pF
Total Gate Charge at V_{DD} = 325 V, V_{GS} = 10 V, I_D = 7 A	Q_g	-	25	-	nC
Gate Source Charge at V_{DD} = 325 V, V_{GS} = 10 V, I_D = 7 A	Q_{gs}	-	5	-	nC
Gate Drain Charge at V_{DD} = 325 V, V_{GS} = 10 V, I_D = 7 A	Q_{gd}	-	11	-	nC
Turn-On Delay Time at V_{DD} = 325 V, V_{GS} = 10 V, I_D = 7 A, R_g = 24 Ω	$t_{d(on)}$	-	45	-	ns
Turn-On Rise Time at V_{DD} = 325 V, V_{GS} = 10 V, I_D = 7 A, R_g = 24 Ω	t_r	-	8	-	ns
Turn-Off Delay Time at V_{DD} = 325 V, V_{GS} = 10 V, I_D = 7 A, R_g = 24 Ω	$t_{d(off)}$	-	35	-	ns
Turn-Off Fall Time at V_{DD} = 325 V, V_{GS} = 10 V, I_D = 7 A, R_g = 24 Ω	t_f	-	31	-	ns
Body-Diode PARAMETERS					
Drain-Source Diode Forward Voltage at I_S = 1 A, V_{GS} = 0 V	V_{SD}	-	-	1.4	V
Body-Diode Continuous Current	I_S	-	-	9	A
Body-Diode Continuous Current, Pulsed	I_{SM}	-	-	35	A
Body Diode Reverse Recovery Time at I_S = 7 A, di/dt = 100 A / µs	t_{rr}	-	334	-	ns
Body Diode Reverse Recovery Charge at I_S = 7 A, di/dt = 100 A / µs	Q_{rr}	-	3.2	-	µC

Electrical Characteristics Curves

Fig. 1 Typical Output Characteristic

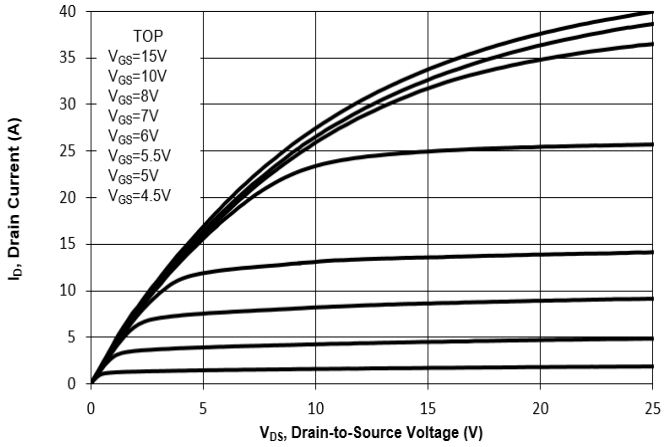


Fig. 2 Typical Transfer Characteristic

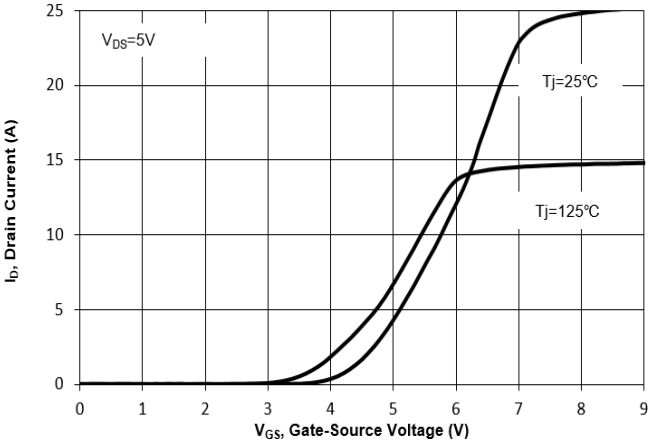


Fig. 3 On-Resistance vs. Drain Current

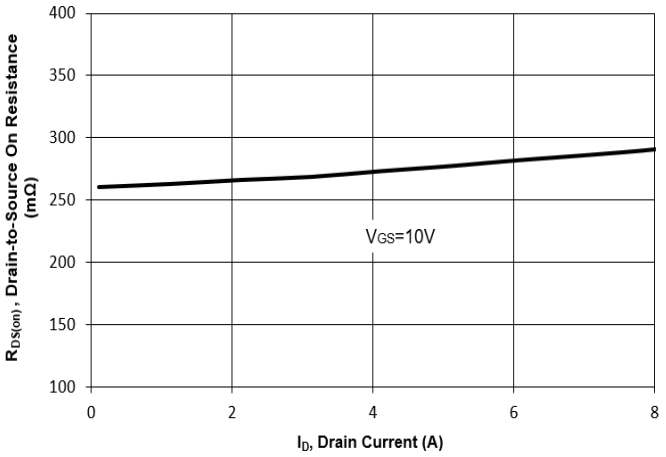


Fig. 4 On-Resistance vs. Gate Voltage

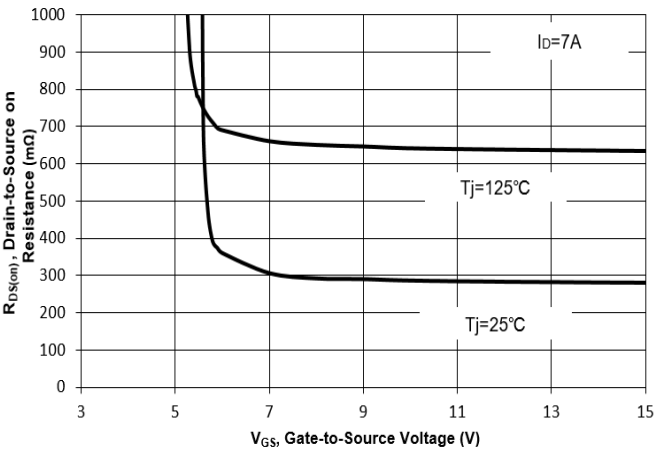


Fig. 5 On-Resistance vs.T_j

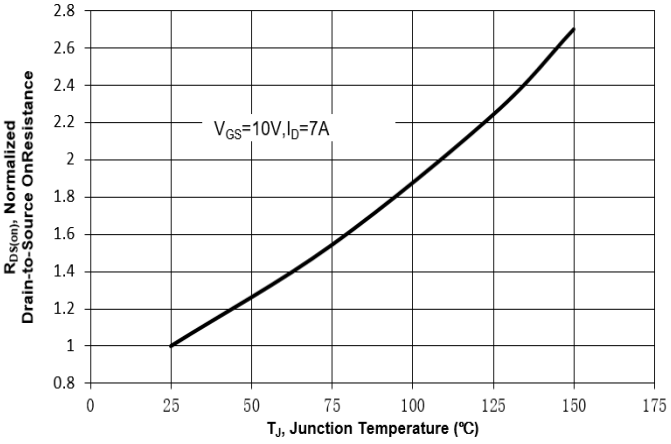
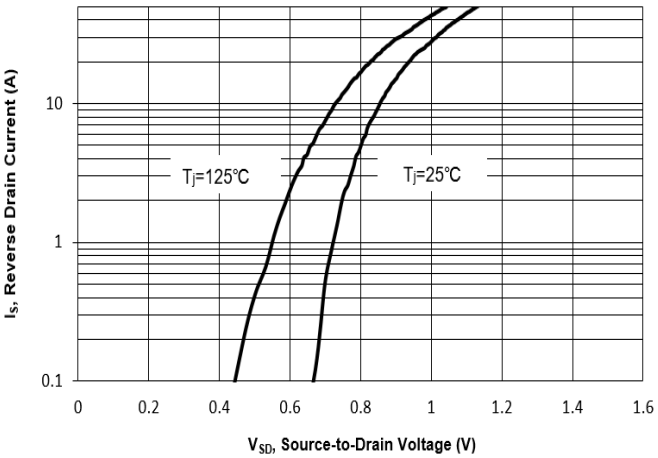


Fig. 6 Typical Body-Diode Forward Characteristic



Electrical Characteristics Curves

Fig. 7 Typical Junction Capacitance

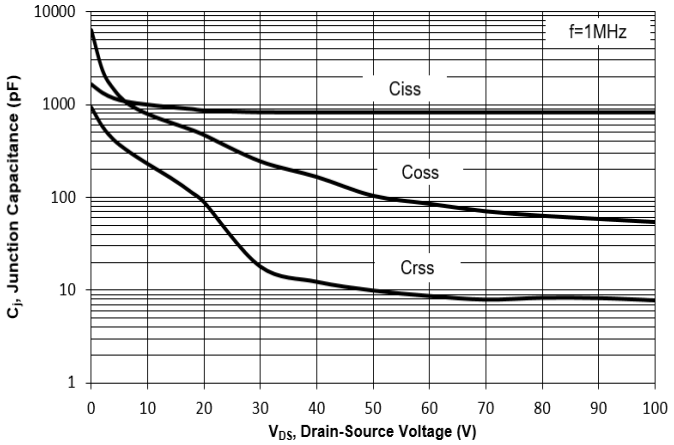


Fig. 8 Drain-Source Leakage Current vs. T_j

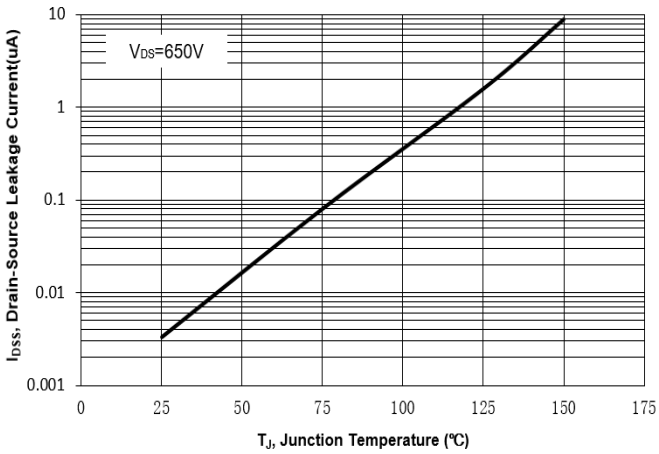


Fig. 9 $V_{(BR)DSS}$ vs. Junction Temperature

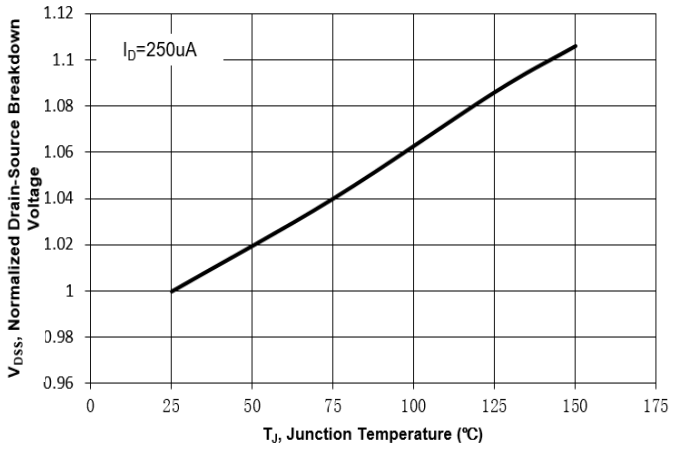


Fig. 10 Gate Threshold Variation vs. T_j

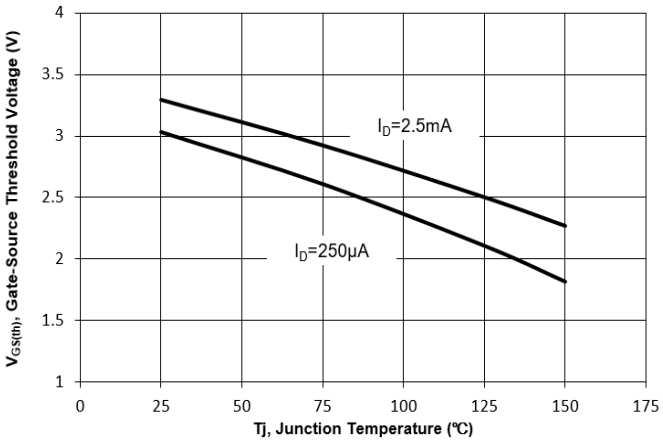


Fig. 11 Gate Charge

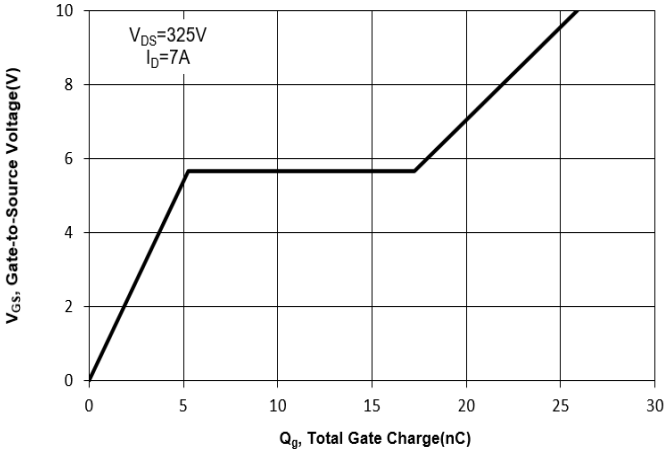
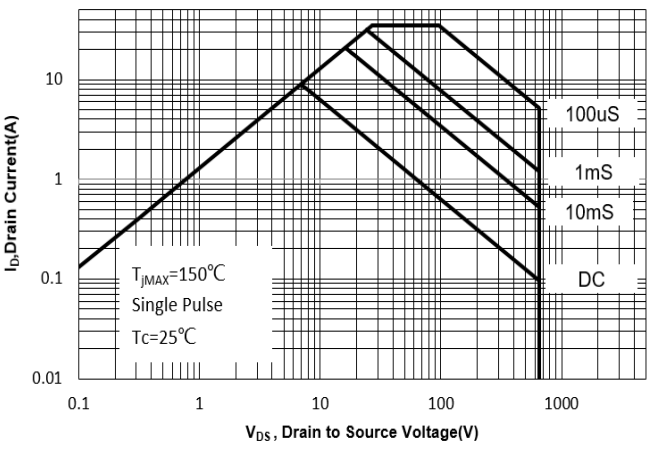


Fig. 12 Safe Operation Area



Electrical Characteristics Curves

Fig. 13 Normalized Maximum Transient Thermal Impedance($z_{\theta JC}$)

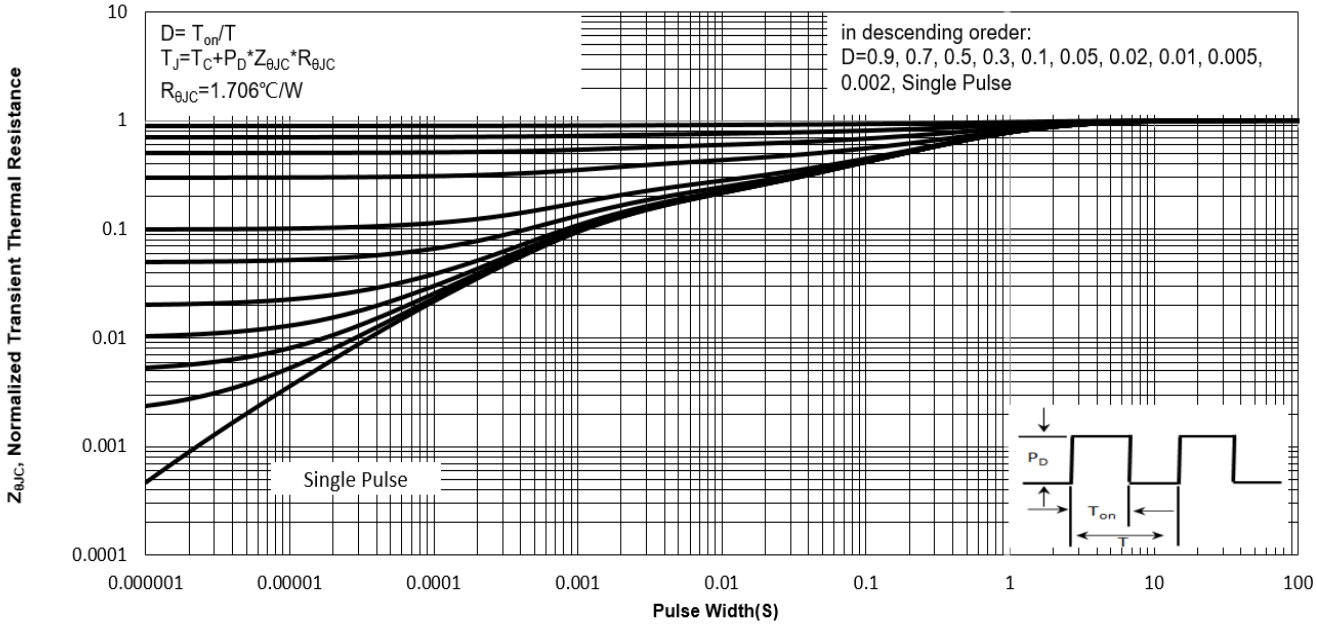
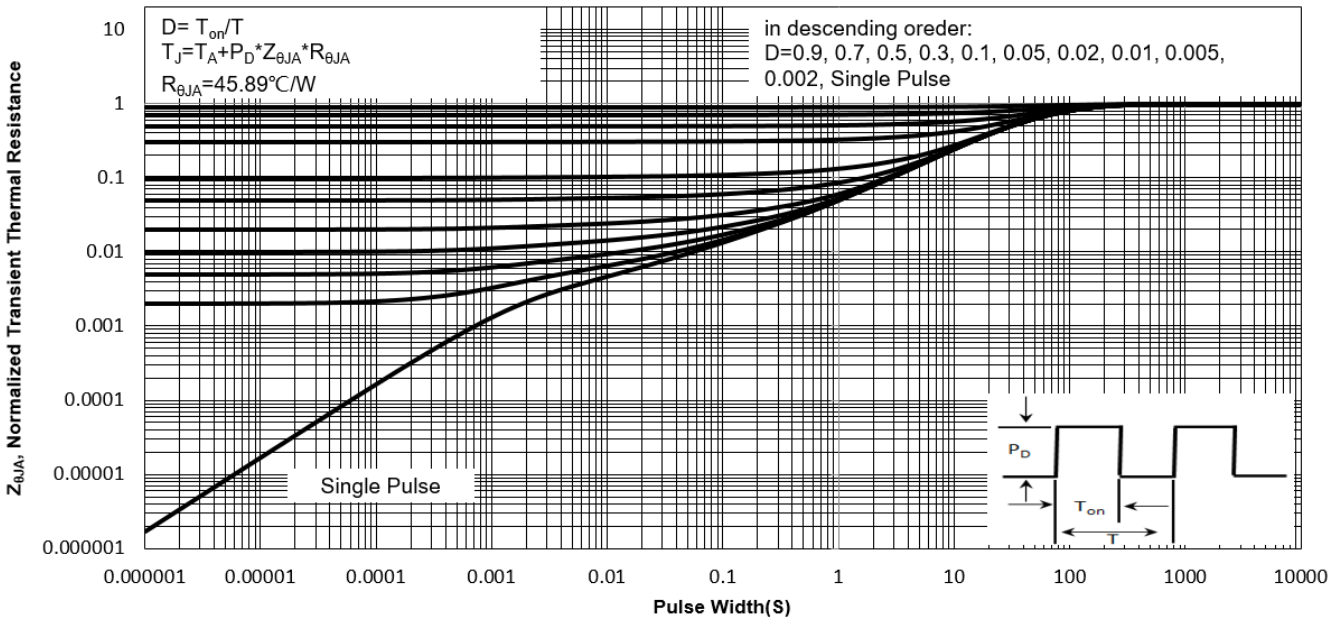


Fig. 14 Normalized Maximum Transient Thermal Impedance($z_{\theta JA}$)



Test Circuits

Fig.1-1 Switching times test circuit

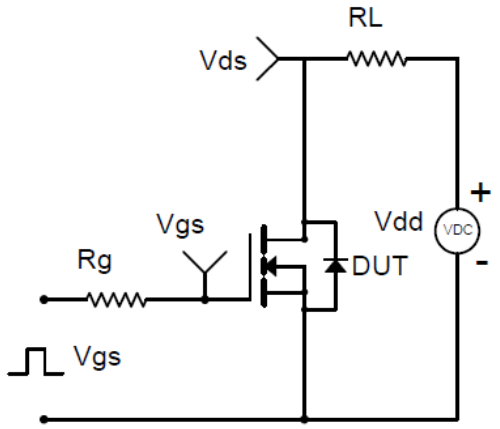


Fig.1-2 Switching Waveform

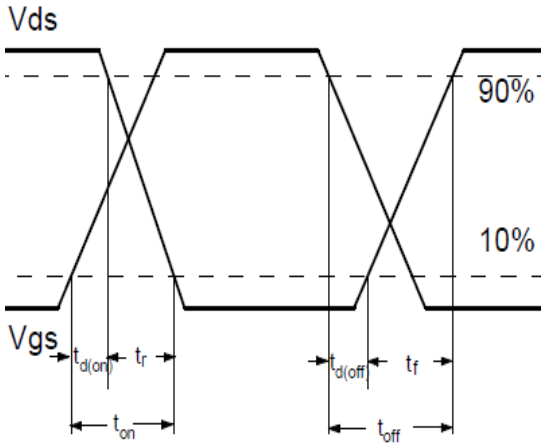


Fig.2-1 Gate charge test circuit

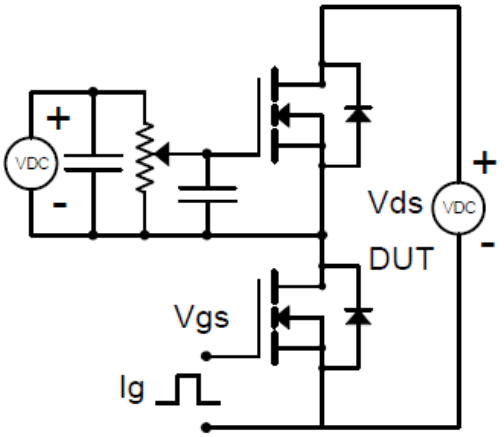


Fig.2-2 Gate charge waveform

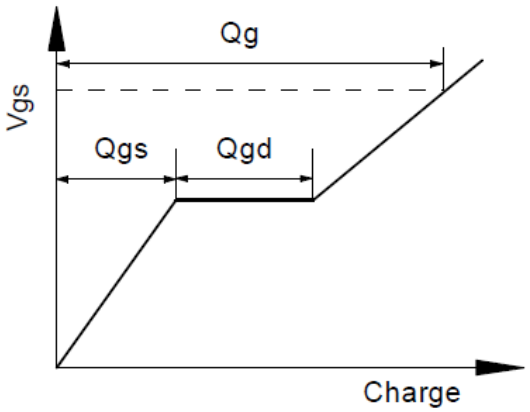


Fig.3-1 Avalanche test circuit

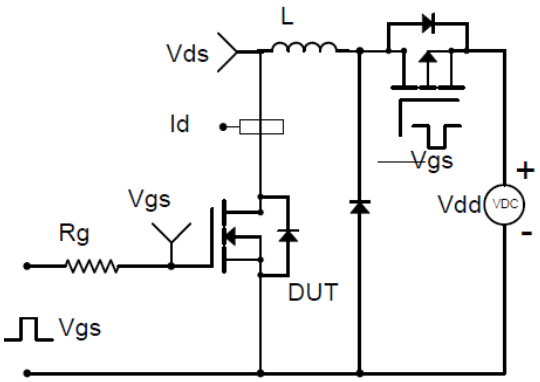
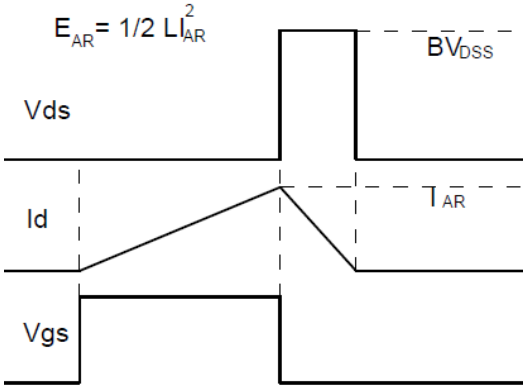
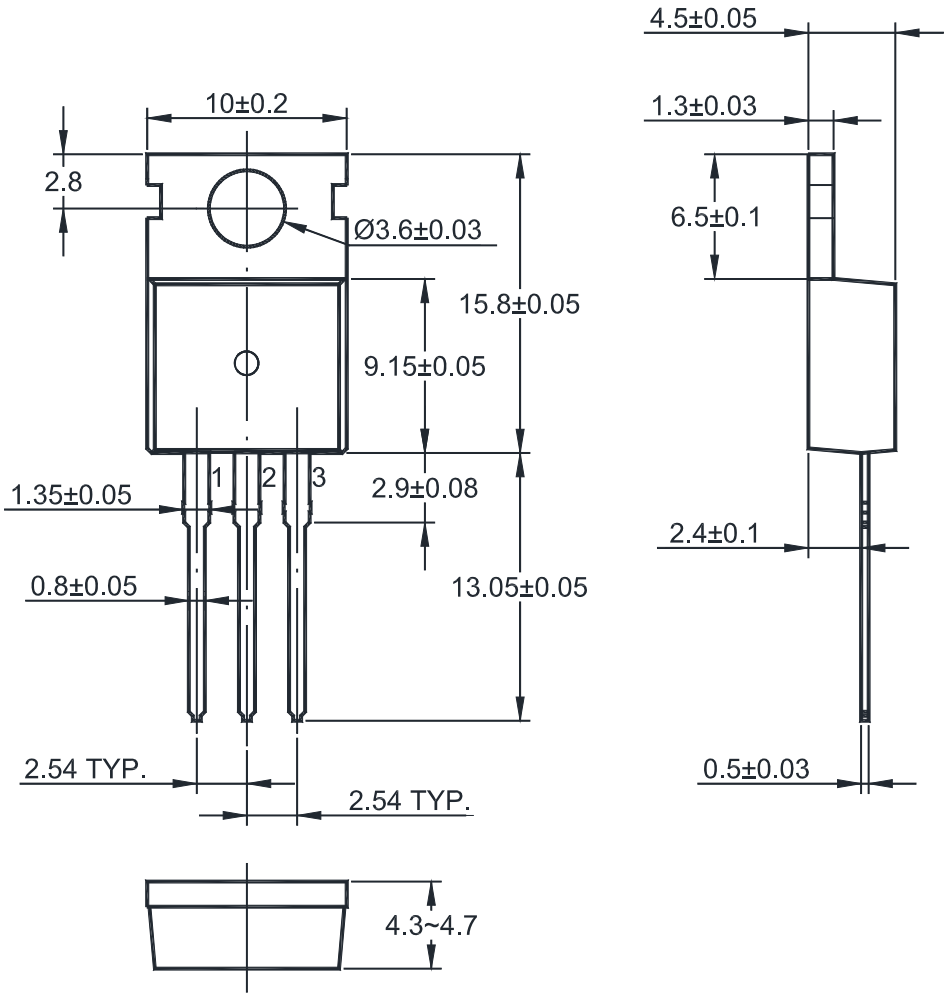


Fig.3-2 Avalanche waveform



Package Outline Dimensions (Units: mm) **TO-220FB**



Marking information

" PCT65N310 " = Part No.
" ****** " = Date Code Marking
Font type: Arial

Winning Team
互創國際

IMPORTANT NOTICE

Our company and its subsidiaries reserve the right to make modifications, enhancements, improvements, corrections or other changes to improve product design, functions and reliability without further notice to this document and any product described herein.

Statements described herein regarding the reliability and suitability of products is for illustrative purposes only. Products specifically described herein are not authorized for use as critical components in life support devices, automobile, military, aviation or aerospace only with the written approval of our company.

The information contained herein is presented only as guidance for product use. No license to any intellectual property rights is granted under this document. No responsibility is assumed by our company for any infringement of patents or any other intellectual property rights of third party that may result from the use of the product.